

TECs and Micro TECs

for Spot Cooling Electronics

In the past decade, modern processors have evolved in both architecture and complexity. Earlier CPUs relied on a single processing core with an ever-increasing clock speed as its major improvement from year to year. This megahertz arms race led us from the 25MHz 486SX to the 3.8GHz Pentium 4 which features a thermal design power level of 115 watts. It was at this power level that traditional low cost air cooling began to approach its limits.

To further increase processing capabilities with each new product launch, a solution was needed to the ever increasing clock speed and its associated thermal tax. This solution was found to be multicore processors that used several smaller and more efficient cores in place of a single core. Modern processor companies, such as Intel and AMD, have produced 4 and 6 core processors that operate in the same thermal envelope as the highest end single core CPUs, with

an order of magnitude higher performance. Some cutting edge companies, such as Tileria, have expanded this idea further with 64 core products and a 100 core processor planned for 2011. The push to parallel processing has given CPUs more capability and efficiency without an overall increase in power dissipation.

At first glance, this microprocessor evolution should make the jobs of system thermal engineers easier. However the complexity of the processor brings a unique set of cooling challenges. As shown in Figure 1, a modern Intel CPU has several processing cores, cache, graphics and a Northbridge controller integrated on a single die [1]. Each of these parts has its own power dissipation and allowable temperature limits. Adding to this complexity, the power dissipation may change dynamically based on the usage, i.e. single versus multi-threaded applications.



Figure 1. A Modern Intel Processor Showing the Integration of CPU, GPU, Cache and Northbridge Controller [1].

Typically, the heat sink on a processor treats the entire die as one discrete heat source. The heat sink base may have multiple heat pipes, or a vapor chamber, but the overall thermal resistance is equal across the die. This approach is simple and low cost, but does not concentrate cooling where needed. A simple heat sink approach must cool the entire die to the temperature of the most sensitive component, which can lead to a larger than necessary design.

A solution to this issue is processor-level spot cooling using integrated thermoelectric coolers (TECs). Thermoelectric coolers are solid state heat pumps which move energy from processor hot spots to a cooling device. A schematic of such a device is shown in Figure 2. Spot cooling with TECs offers several advantages which must be carefully studied to ensure a successful implementation. Several companies are conducting research and producing TECs for this application. One of these, Nextreme, offers the following information on the application of TEC spot cooling [2].

Localized micro TEC-assisted heat conduction provides a new design element for power management.

An increase in temperature creates lifetime and reliability problems for integrated circuits. There are many possible temperature-dependent failure mechanisms for integrated circuits. One example is failure due to electro migration. In this case, the lifetime of an integrated circuit depends exponentially on its temperature, according to the model of Black:

$$\tau = \frac{C}{J^2} \exp\left(\frac{E_a}{k_b T}\right) \quad (1)$$

Where, τ is the mean time to failure, C is a proportionality constant, J is the current density, k_b is Boltzmann's constant, and T is the absolute temperature. E_a is activation energy, where the typical value for silicon is about 0.68 eV. Accordingly, device reliability depends on maintaining T below acceptable levels for all the circuits in the chip.

Higher temperatures compound thermal management problems by increasing overall power consumption due to increased sub-threshold leakage. The off-state sub-threshold leakage current in transistors is becoming a major

contributor to total power dissipation as feature size drops. Even today, this static power dissipation is becoming a limiting factor in low power designs. The projected power consumption from sub-threshold leakage exceeds the total dynamic power consumption as the technology drops below the 65 nm feature size [3].

Leakage current in a transistor occurs across the gate to the drain (mitigated by high dielectric constant materials) and from the source to the drain (mitigated by lowering the supply voltage or raising the threshold voltage, V_{th}). As a result, designers have reduced supply voltages to below 1 V and are using multiple V_{th} as well. Areas of the chip built with high V_{th} have reduced leakage, but sacrifice operating frequency. It takes the transistors a longer time to turn on with a reduced voltage difference between the supply and V_{th} . Areas of the chip with lower V_{th} have higher speed, but higher leakage as well. Because sub-threshold leakage current is activated by temperature (and, therefore, increases rapidly with rising temperature) cooling hot regions of the chip may actually result in reduced total power consumption.

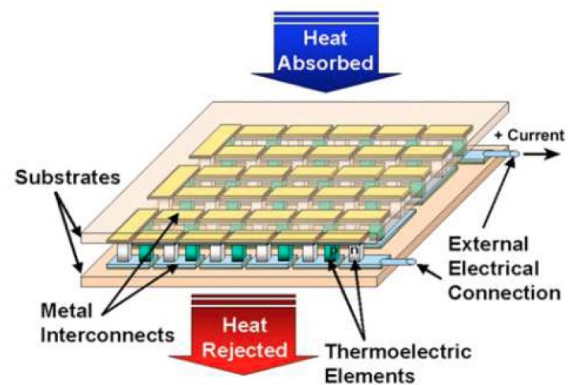


Figure 2. Detailed View of a Thermoelectric Cooler [2].

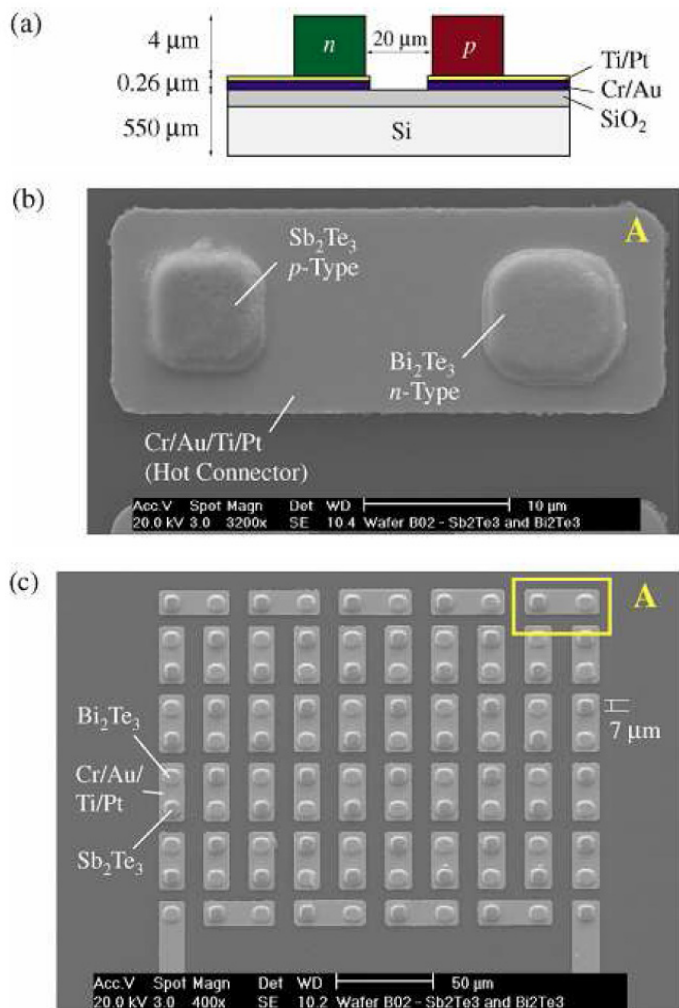


Figure 3. Micro Thermoelectric Cooler Structure [3].

da Silva et al [3] have investigated the fabrication and performance of micro thermoelectric coolers. Figure 3 shows the schematic design of a micro TEC. Reference [3] states that thermoelectric cooling is a suitable technique for the local cooling of micro-sensors and devices because it does not require any moving parts and can be micro-electronically integrated. While the search for thermoelectric materials compatible with solid-state electronics material continues, tellurium compounds currently have the highest cooling performance around room temperature. Micro TECs are fabricated by vapor deposition of tellurium compounds on a very low thermal conductivity SiC membrane to minimize the heat leakage effect.

As processor design becomes more complex and more functions are integrated into CPUs, the need for spot cooling will continue to increase. Today, air cooling is being pushed to its limits in many applications, and spot cooling is a viable alternative to liquid cooling. However, several improvements need to be made before this can happen. The current research and development in this field must produce TECs with increased efficiency and lower cost for them to find widespread adoption in the market.

References:

1. Sandy Bridge Presentation, Intel Corporation, Computex, June 2010.
2. Snyder, J., Soto, M., Alley, R., Koester, D. and Conner, B., HotSpot Cooling Using Embedded Thermoelectric Coolers, Nextreme Thermal Solutions, SEMI-THERM 22, 2006.
3. daSilva, L., Kaviany, M., DeHennis, A. and Dyck, J., MicroThermoelectric Cooler Fabrication: Growth and Characterization of Patterned Sb₂Te₃ and Bi₂Te₃ Films, University of Michigan, 2004.



**First Volume of
Qpedia Thermal
eMagazine
Articles Now
Available in
Hardcover Book!**

ATS has published Qpedia Thermal eMagazine, Volume 1, Issues 1-12, a hardbound, full-color book that compiles 46 technically comprehensive articles offering expert-level coverage on a wide range of heat management issues that impact virtually all of today's electronic devices.

Qpedia Thermal eMagazine, Volume 1, Issues 1-12, ISBN-978-0-615-23660-5, the hardbound, full color book can be ordered for \$94.95 (USD) by calling 781-769-2800 or by email Qpedia@qats.com. Contact ATS or visit www.qats.com/qpedia.asp for details.