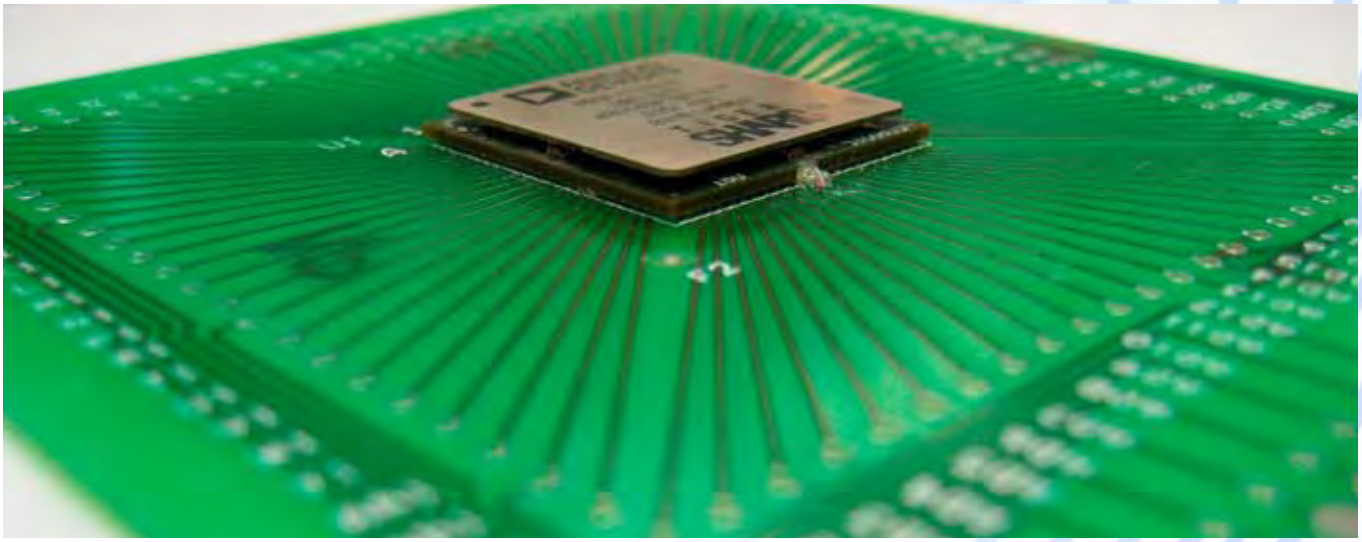
Understanding the JEDEC Integrated Circuit Thermal Test Standards



The primary goal of thermal engineering in electronics cooling is to reduce the junction temperatures of IC devices. Defining the thermal resistance is a common approach to determining junction temperature, given a set of environmental conditions and a component's power dissipation. However, this approach would only be meaningful if all suppliers used the same standard test methodology to determine thermal resistance of semiconductor devices.

The entity that has taken on the task of establishing benchmarks in the electronics industry is the JEDEC Solid State Technology Association. This trade group, originally the Joint Electron Device Engineering Council, is the semiconductor standardization body of the Electronic Industries Alliance (EIA) and represents all areas of the electronic industries.

JEDEC has 50 committees and subcommittees, all of which are overseen by the JEDEC Board of Directors. Members of JEDEC committees come from 290 companies that are active in the semiconductor industry sector, either as manufacturers or users of semiconductor components.

JEDEC standards are accepted worldwide. The main purpose of JEDEC standards and publications is to protect the public interest by eliminating misunderstanding between manufacturers and purchasers, and by facilitating the interchangeability and improvement of products. Another function of these standards is to assist JEDEC nonmembers to select and obtain proper products with minimum delay [1].

JESD51 provides an overview of the methodologies for the thermal measurement of packages containing single chip semiconductor devices. The actual methodologies are distributed among several documents which can be selectively used to meet specific thermal measurement requirements.

A brief description of the complete JEDEC51 family of standards is presented in Table 1.

Table 1. JEDEC Thermal Measurement of IC Package Standards [2].

Standard	Description
JESD51	Overview of methodology for thermal testing of single semiconductor devices
JESD51-1	Test method to determine thermal characteristics of a single IC device
JESD51-2	Test method to determine thermal characteristics of a single IC device in natural convection (s
JESD51-3	Thermal test board design with a low effective thermal conductivity for leaded surface mount packages
JESD51-4	Design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages.
JESD51-5	Thermal test board design for packages with direct thermal attachment mechanism
JESD51-6	Test method to determine thermal characteristics of a single IC device in a forced convection
JESD51-7	Thermal test board design with high effective thermal conductivity for leaded surface mount packages
JESD51-8	Environmental conditions for a measurement of Junction-to-board Thermal resistance
JESD51-9	Thermal test board design for Ball Grid Array (BGA) and Land Grid Array (LGA)
JESD51-10	Thermal test board design for Dual-Inline Packages (DIP) and Single-Inline Packages (SIP)
JESD51-11	Thermal test board design for Pin Grid Array (PGA) packages
JESD51-12	Guidelines for reporting and using Electronic Package Thermal Information

In JEDEC standards, thermal characterizations of a semiconductor device require measurement of the junction. There are a number of methods to measure the die temperature, such as infrared and liquid crystal sensing, but the most commonly used is the voltage drop across a forward-biased diode. This diode is specifically designed into the thermal test die and in many integrated circuit devices. The measurement current through the test diode must be large enough to not be influenced by surface leakage, yet not small enough to cause considerable self-heating.

A typical value for measurement current is from 100 µA to 5 mA, depending on the size of the diode [1].

Under JEDEC standards, there are two approaches to measuring the junction temperature. One is known as **Static Mode**, where heating power is continuously applied to the Device Under Test (DUT) while monitoring the junction temperature. This method is suitable for use with thermal test diodes and some active integrated circuit devices. The other approach is referred to as **Dynamic Mode**, during which power is applied to the DUT for a specific period of time to reach equilibrium, and then switches to measurement mode. This method is suitable for most active integrated circuits [1].

Thermal characterization of a semiconductor that is generated using JESD51 standards is defined as thermal resistance and is governed by Equation 1:

$$\theta_{JX} = \frac{T_J - T_x}{P_H} \quad (1)$$

In the above equation, θ_{JX} is the thermal resistance from device junction to the specific environment (°C/W), T_J is device junction temperature (°C), T_x is the reference temperature for the environment (°C) and P_H is the power dissipated in the device (W).

Another definition used in JEDEC standards is the Thermal Characteristic Parameter, and is governed by Equation 2:

$$\psi_{JX} = \frac{T_J - T_x}{P_H} \quad (2)$$

The main difference between θ_{JX} and ψ_{JX} is that the thermal resistance θ_{JX} is calculated in a condition where nearly all of the component power dissipation flows through either the top or the bottom of the package. On the other hand, in calculating the Thermal Characterization Parameter, power is the total power dissipation in the chip and may leave the chip through any thermal path, not just from the top or the bottom of the package.

It must be noted and emphasized that both thermal resistance and thermal characterization parameter values can be used to compare different packages and estimate how a package will perform in a specific application. However, these estimates cannot be accurate because a standardized test condition will not match the user's application.

To determine thermal values of semiconductor devices, a number of temperature measurements must be taken. Figure 1 shows the locations of these measurements on a single chip.

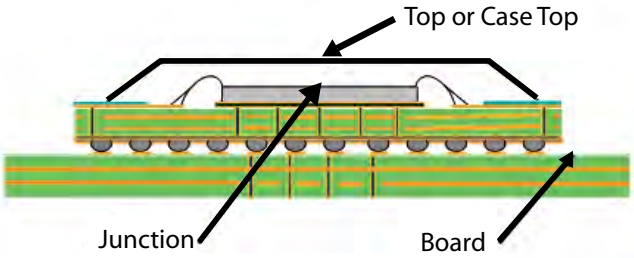


Figure1. Typical Temperature Location Designation [3]

As seen in Table 1, there are 12 standard documents related to thermal measurement of component packages. In this article, however, only a few of these standards are briefly explained.

JESD51-2

This standard specifies guidelines for determining the thermal characteristics of a single device in a natural convection condition (still air). The methodology calls for construction of a test fixture and a 30 x 30 x 30 cm (cubic foot) enclosure in which measurements are taken. The environmental conditions are pertinent to surface-mount packages mounted on a standard test board. The board is placed in a horizontal position, package up, in an enclosure that prevents extraneous air currents and allows only natural convection. The junction-to-ambient thermal resistance for this condition is designated by and is calculated from Equation 3, which is similar to θ_{JA} Equation 1 where the specific reference environment is taken as ambient [4].

$$\theta_{JA} = \frac{T_J - T_A}{P_H} \qquad (3)$$

JESD51-2 also includes a guideline that determines the thermal characterization parameter ψ_{JT}, from the junction to the top center of the package. This useful value allows estimation of the junction temperature and is calculated from Equation 4. This equation is the same as Equation 2, where the specific reference environment is taken as top center of the device package.

$$\psi_{JT} = \frac{T_J - T_T}{P_H} \qquad (4)$$

JESD51-6

This standard specifies the environmental conditions for determining the thermal characteristics of an IC device in forced convection. The standard includes specifications for a wind tunnel that must be used.

The most important of these wind tunnel specifications is the flow uniformity, with flow fluctuation not exceeding ±5% of the mean velocity across 90% of the test chamber cross-section or ±5% along the length of the test section. Another specification is the swirl of the mean flow, which must be less than 5% of the mean flow velocity. Flow swirl is measured with a three axis or cross wire anemometer capable of measuring flow in at least two directions [5].

This standard also specifies guidelines for the placement of the IC in the test section of a wind tunnel. The IC package is mounted on a test board, as specified in JESD51-3 and JESD51-7, and can be placed in the test chamber section of the wind tunnel in different flow-board orientations, [5], Flow velocity must be measured upstream of a device with an anemometer with a reading accuracy of ±4%. Ambient temperature must be measured with a calibrated thermocouple with a wire diameter no larger than 0.5 mm [5].

Junction-to-air thermal resistance is designated by θ_{JMA}, which is the resistance from the junction to the moving air. Its definition is similar to Equation 1, with the specific reference environment taken as the moving air.

Another useful resistance value in this standard is junction-to-board thermal characterization parameter ψ_{JB}, which is defined by Equation 5.

$$\psi_{JB} = \frac{T_J - T_B}{P_H} \qquad (5)$$

JESD51-8

This standard offers guidelines for obtaining the junction-to-board thermal resistance of an IC mounted on a high-conductivity board as specified in JESD51-7. The resistance is defined in Equation 6, and indicates the resistance of heat spreading horizontally between the junction and the board. The board temperature is taken near the board surface on one of the package's center traces.

$$\theta_{JB} = \frac{T_J - T_B}{P_H} \qquad (6)$$

In order to transfer nearly all of the heat to the board, a ring-style copper cold plate is used. The package openings in the top and bottom of the cold plate are insulated. The cold plate is clamped onto the solder mask-covered traces on the board at a minimum of 5 mm from the package. The cold plate clamp area must be a minimum of 4 mm wide. The incoming cooling fluid should be controlled at the ambient room temperature in a range of +2 to -5°C [6].

A schematic of such a cold plate is shown in Figure 2.

Junction-to-Case Resistance

Even though measurements of θ_{JC} have been common for years, JEDEC does not yet have a covering standard. It is very difficult to define a measurement method that provides accurate and repeatable results covering a wide range of package designs, sizes, and power dissipation. The development of a JEDEC test method to measure θ_{JC} is in the works [3].

The JEDEC-51 family of standards has allowed manufacturers of semiconductor devices to report thermal information in a consistent manner. This has enabled end users to properly understand, interpret, and use the data reported. One particular discipline to benefit from these standards is thermal engineering. JEDEC thermal standards have empowered thermal engineers to use reported data to thermally characterize IC devices and to design and develop products that manage and maintain heat within a safe range. This not only substantially prolongs the life of electronic components, but as the technology advances, allows faster devices with higher heat output to be designed and implemented.

References:

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5. EIA/JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air), March 1999.
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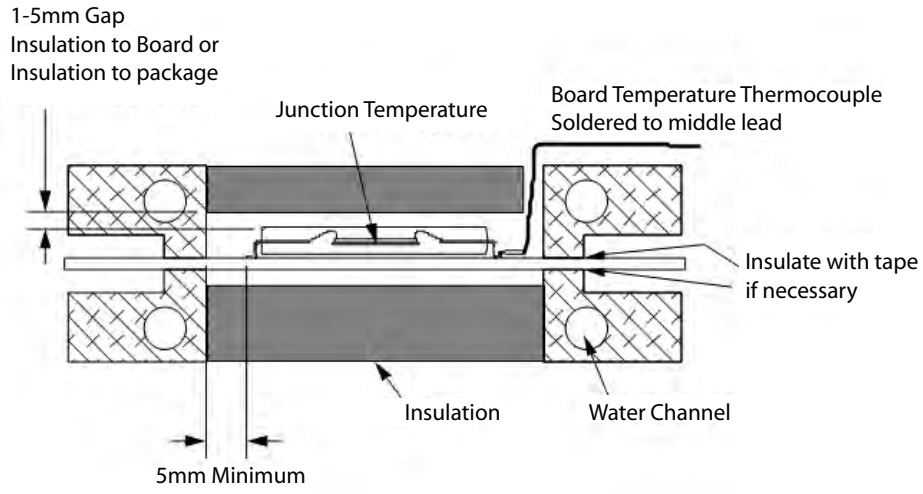

Figure 2.
Illustration of Ring-Style Cold Plate Θ_{JB} Test Fixture in Cross Section [6].