JEDEC: Review Of Standards

On Compact Thermal Modeling

At the time when a gallon of gas was $.25 and the integrated circuit was deemed “invented”, an organization was formed known as JEDEC. The Joint Electron Devices Engineering Council is now made up of more than 3,000 volunteers from nearly 300 companies around the globe. The 50+ committees have a common vision: to create an evolving set of standards to ensure product interoperability, reduce cost and time to market. As a result, companies can base their designs on a set of standards and focus more on R&D. The resulting benefit is less time invested on product invention and more on innovation.

To maintain consistency with **Qpedia**, this article will focus on the thermal management of electronics and the JEDEC standard JC-15: Thermal Characterization Techniques for Semiconductor Packages. The scope of JC-15 includes the standardization of thermal characterization techniques, both testing (JESD51) and modeling (JESD15), for electronic packages, components and materials for semiconductor devices. For a closer look at standard JESD51 and the Thermal Measurement Methods of an Integrated Circuit, please look through the **Qpedia** archives and review an article in the June, 2007 issue titled: “Understanding the JEDEC Integrated Circuit Thermal Test Standards”.

The electronic industry has evolved such that new components are outperforming their predecessors. Packages are outputting more power, yet getting smaller in size, and operating at increasing temperatures. As we know in Thermal Engineering and as a Provider of Heat Sinks at Advanced Thermal Solutions, insuring that components are operating within the specified range is usually the last thing thought of when bringing new products through the design phase. These are highly 3D problems; insomuch as, in addition to the power of the devices, there can be increases in temperature due to the environment such as airflow characteristics, thermal coupling of neighboring devices, system altitude, etc. All possibilities must be taken into account when looking at how the entire system will operate.

When looking at a system, the greatest points of concern are the Junction Temperatures (T_j). As defined by JEDEC: “Absolute maximum rated junction temperature is the maximum junction temperature of an operating device, beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology” [1]. Figure 1 shows the junction location and an example of how a semiconductor can be packaged and installed onto a PCB.

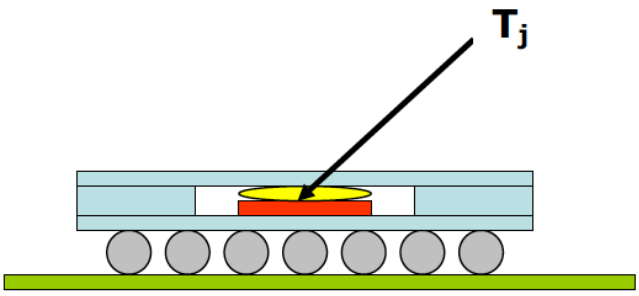


Figure 1 – Package Attached to PCB via BGA

During operation, The T_j must be monitored and maintained within the range specified by the device manufacturer. This is because temperatures outside the range speed up chemical reactions and accelerate changes in materials. This produces distortion stress on the junction between

two materials with different expansion rates. If this occurs repeatedly, material fatigue arises, causing failures such as hermetic seal damage, die bond adhesion damage and bonding wire opens. In addition, if the device is used with improper connections, the heat generated from the equipment or element can accelerate the temperature change and affect the product in an accelerated manner. [3]

The ranges differ per application; for example, the temperature range of a Xilinx Spartan -6 FPGA is:
C = Commercial (T_j = 0ºC to +85ºC)
I = Industrial (T_j = -40ºC to +100ºC)

Xilinx denotes this range in the item number by ending with a "C," or an "I." Check your own device manufacturer for the operating range for your application i.e., Commercial, Industrial, or Military.

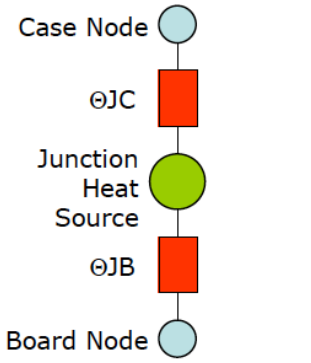
For users to maintain a safe T_j, we must know the semiconductor's thermal resistance. Due to the fact that semiconductors need to perform in a wide array of environmental (surroundings, mounting, etc.), electrical (power levels, currents, voltages, etc.) suppliers must adhere to a standardized approach to defining the thermal resistance. It is by these means that both the manufacturer and the user can determine an accurate T_j.
Thermal modeling is constantly becoming more significant in the characterization of components and for predicting T_j for standard testing, as well as within the applications environment. The resulting data can be used by design engineers in evaluating the package itself, its reliability and to analyze the thermal performance of the entire system.
Due to the complexity of system level analysis, engineers would sometimes be constructing simulations with a lack of information. This resulted in an increased time investment to create an accurate model. Because of this, JEDEC decided that it made more sense for the suppliers themselves to characterize their own products for end users. There are several benefits to this approach. One major benefit is that the suppliers protect themselves by ensuring the accuracy of the thermal performance of their products and models released to their customers. In addition, if the models were said to be performed by the user, the supplier would lose any control over the accuracy of the data resulting from simulation.

JEDEC has introduced to the standards, Compact Thermal Models (CTM), to insure accuracy and compatibility throughout the industry, while providing a way for suppliers to share data effectively with global customers. A CTM is a way to "hone— in" on the component package and achieve a high level of boundary condition impedance (BCI), so that the thermal behavior of that component can be supplied for system level simulation. There are two methods defined by JEDEC, they are: The Two Resistor Model, and The DELPHI Model. These models are described below and are illustrated in Figures 2 and 4; but, first, let's look at the properties and assumptions that were made when creating these models:

Properties:
• Limited Complexity (10's of Nodes)
• Vendor/Software Neutral
• Adaptable to mainstream conduction codes for package-level thermal analysis
• Capable of insertion into standard numerical codes for system/board-level analysis
• Absolute BCI property is when CTM calculates chip temperature in all possible environments in agreement with results of detailed model calculation
• Fully documented, nonproprietary

Assumptions:
• Package contains single IC with each node representing a single temperature region
• Package mounted to a PCB
• Heat flows from the chip package to the:
– Top surface to ambient fluid or heat sink
– Side surfaces to ambient fluid
– Bottom surface / leads to PCB
• Thermal resistor networks are used to represent heat flow paths
• External surfaces can either be:
– Considered isothermal and represented by single nodes
– Subdivided into isothermal regions with corresponding nodes

As engineers, we can apply the Two-Resistor Model at different points of the design process. At first, the model may be used as an upfront calculation to see how the component/package may behave. Further into the design process, the model may be assimilated into a more detailed model using Computational Fluid Dynamics (CFD) software.



Represents heat flow from device to a heat sink—ambient fluid, from device to bottom surface—PCB.
Side Surfaces ignored

- Junction to board/Case resistance is measured using:

$$\Theta Jx = (TJ - Tx)/PH$$

- Thermal characterization parameter (optional) is measured using:

$$\Psi Jx = (TJ - Tx)/PH$$

When Modeling:

$$\Theta = 1/hA$$

Case-to-ambient resistances depend on environmental conditions

- if bare: use data from table 1
- if heat sink is attached use resistance values

Figure 2 - Two Resistor Model

Cooling Regime	Approximate Heat Transfer Coefficient Range (W/m^2K)
Natural Convection, Air	2—30
Forced Convection, Air	15—3000
Forced Convection, Water	200—10,000
Pool Boiling, Water	3,000—50,000

Table 1 - Typical cooling regimes in electronics [4]

The Two-Resistor Model consists of three nodes connected by two thermal resistors. These represent the measured values of the Junction - Board (Θ_{JB}) and Junction - Case (Θ_{JC}) resistances as seen above, with the Board Node considered in direct thermal contact with the PCB under the package and the Case Node in direct contact with the environment atop the package. Typically, what is in contact with the top of the package is air or a thermal interface material in conjunction with a Heat Sink as seen in Figure 3. A heating power is then applied to the Junction node. In this model the heat flows in only two directions. No heat flow through the sides is accounted for.

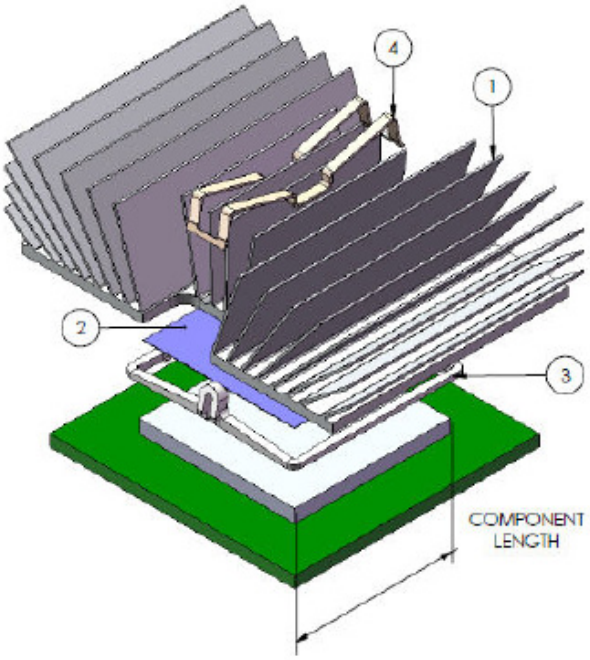


Figure 3 - maxiFLOW/superGRIP™ Heat Sink with Thermal Interface Material

As noted, care should be taken because the model doesn't consider environmental conditions, and these must be specified by the engineer at the Case and Board nodes. Furthermore, the error bounds cannot be determined from the generation of the model. They may be derived from comparing the engineer's predictions with data from actual tests.

As technology has evolved, the use of 3D simulation tools has become nearly standard. Using programs such as CFDesign™, and 6sigmaET™ can solve both the solid and air portions of the system directly. This is done by solving the Navier- Stokes equations which govern fluid flow and heat transfer. There is error in this method as well, as the program has to converge to a number. When setting up the CFD tool, care should be taken to ensure the correct interaction it will have with the surrounding flow. This is done by maintaining the physical geometry of the package. [4]

Table 2 shows the process flow for a thermal network and a 3D simulation approach to the Two-Resistor Model.

Conduct the ΘJB and ΘJC tests and extract metrics.	Generate as close to actual size and profile
ΘJB unavailable → Calculate and use ΨJB	Use software to construct two-resistor network
Report metrics, package power and geometry → Height, exposed top area, area contacting PCB	Verify the correct heat dissipation is introduced
Report emissivity of exposed package surfaces	Assign emissivities to all correlating surfaces
	Ensure that the sides are insulated so that heat is only transferred through the top and bottom of model

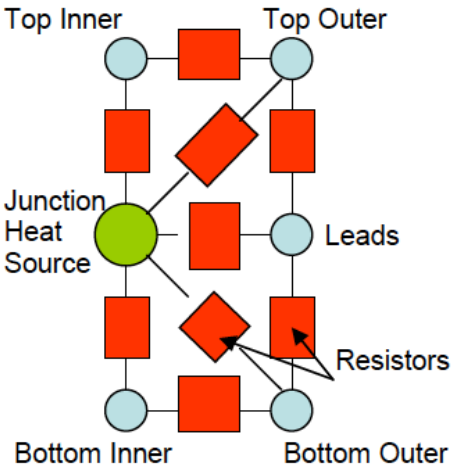
Table 2 - Thermal Network and 3D Simulation Methods

Even though less accurate, the intuitiveness and simplicity of the Two- Resistor model makes it attractive for engineers to construct. For a more complex and accurate approach, we shall look to the DELPHI project.

Much can be claimed by The DELPHI project. It is in fact, DELPHI (**DE**velopment of **L**ibraries of **PH**ysical models for an **I**ntegrated design environment) that coined the term "Compact Thermal Model" (CTM) and started the movement to establish standard methods of usage and sharing of component characterizations. After 1996, subsequent projects such as SEED (**S**upplier **E**valuation and **E**xploitation of **D**ELPHI) and PROFIT (**PR**ediction **OF** **T**emperature Gradients Influencing the Quality of Electronic Products) further develop publically the CTM, while members of each organization maintain their activity within JEDEC.

A DELPHI compact model is a thermal resistance network. This CTM is comprised of a limited number of nodes connected to each other by thermal resistor links (see Figure 4). With knowledge that the thermal problems are highly 3D, the heat flow within a component/package is represented in the model by a series of links. Network nodes are, by definition, each associated with a single temperature only. The nodes can be either surface or internal.

Surface nodes are associated with a physical region of the package surface defining the area of the node. In such a case, the nodal temperature represents the average temperature of the area allocated to the node in the actual package. Also, surface nodes must always have a direct one-to-one association with the corresponding physical areas on the actual package. Therefore, it is critical that they communicate with the environment in the same manner as the package. [5]



Temperatures averaged. Nodes communicate with each other. Surface nodes with environment, internals may have a heat source associated with them

- Objection function formulation:

$$F = \sum_{1}^{M} \left\{ W \left(\frac{T_{J,C} - T_{J,D}}{T_{J,D} - T_{Amb}} \right)^2 + \left(\frac{1 - W}{N} \right) \sum_{i=1}^{i=N} \left(\frac{q_{i,C} - q_{i,D}}{Q} \right)^2 \right\}$$

- where:
- F objection function
- M # boundary condition sets ("38 set")
- W weight factor (.5 balances flux & temp)
- N external nodes
- TJ,C junction temperature compact model
- TJ,D junction temp detailed model
- TAmb ambient temp
- qi,C flux leaving ith node (compact model)
- qi,D flux leaving ith node (detailed model)
- Q total power applied to the junction

Figure 4 - DELPHI Model

The objection function is the difference between the detailed model and the compact model summed over the boundary condition set and a finite number of points within the component package. [5]

Minimizing the Objection function should result in a compact model that has a low error. Table 3 illustrates the generation flow for DELPHI model generation.

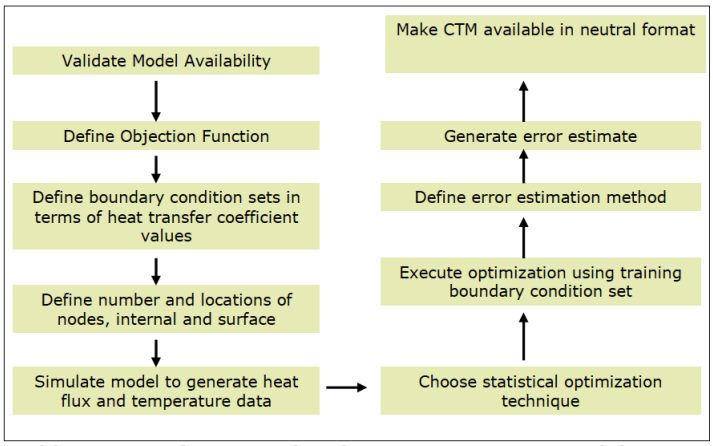


Table 3 - Steps in Generating the DELPHI Compact Model.

It is important to keep in mind that the availability of the DELPHI compact model does not eliminate the need for understanding the application in which the package is to be used. In other words, it is the user's responsibility to take into account the environment surrounding the package. The environmental conditions for the relevant application must be applied at the surface nodes as boundary conditions. [5]

There are a number of criteria that have been established to provide a comparison of the CTM methods. Table 4 shows the Criteria and the Application of it for each Model.

Two Resistor Model	DELPHI Model
• Is it test or simulation based?	
Test. The resistors are extracted from standard thermal tests or a validated model that simulates the test environment	Simulation. The resistor values are chosen by minimization of the Objective Function
• Does it contain an artifact from the test environment?	
Yes. There is a contribution due to heat flow through test board (note thermal conductivity—use 2s2p board)	No. Resistance for heat flow in the test board is neglected.
• Is there an error analysis included in methodology?	
No. Not in a two-resistor CTM	Yes, due to the statistical procedure used to extract optimum values for the resistors.
• Calculation of BCI and BCS Indices	
– Intended to provide comparison of accuracy between alternate methods	
– Supplier is requested to disclose calculated values of BCI and BCS Indices	

Table 4 - CTM Criteria – Comparison

The objective of the Compact Thermal Models, as described, is to simplify a component or package, verify its thermal performance and install the findings into a system, and perform simulations to determine thermal behavior within relevant applications. It has been in the best interest of suppliers to construct these CTMs and validate their products so that users shall have confidence in the capabilities of those products. The electronics cooling industry is much like fashion, in that: what may be successful today, will be unworkable or impractical tomorrow. JEDEC and its application of the CTMs are constantly evolving with the innovation of simulation tools, components and their applications. Within an ever changing marketplace, JEDEC standards advocate increases in reliability, interoperability, cost reduction and decreases in time-to-market for products within the microelectronics industry.

References:

1) JEDEC Standard, JESD22-A108D, June 2005, "Temperature, Bias, and Operating Life." <http://www.jedec.org/standards-documents/docs/jesd-22-a108c>

2) Xilinx, March 21, 2011, "Spartan-6 Family Overview" <http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf>

3) Toshiba Corporation, July 2010, "Operating Environment Factors." <http://www.semicon.toshiba.co.jp/eng/product/reliability/device/concept/1186220_7655.html>

4) JEDEC Standard, JESD15-3, July 2008, "Two-Resistor Compact Thermal Model Guideline." <http://www.jedec.org/sites/default/files/docs/JESD15-3.pdf>

5) JEDEC Standard, JESD15-4, October, 2008, "DELPHI Compact Thermal Model Guideline." < http://www.jedec.org/sites/default/files/docs/JESD15-4.pdf>